WHAT IS CLAIMED IS:

1. A semiconductor memory comprising:

a memory cell array having a memory cell;

a sense amplifier to read/write data from/in the memory cell array;

a pair of bit lines to connect the memory cell to the sense amplifier;

a bit line equalizer to equalize potentials of the pair of bit lines; and

a sense amplifier equalizer to equalize potentials of two power supply nodes of the sense amplifier,

wherein the sense amplifier equalizer comprises MOS transistors whose gate oxide films have different thicknesses.

2. The memory according to claim 1, wherein the sense amplifier equalizer is controlled by control signals having different logic amplitudes in correspondence with the MOS transistors.

3. The memory according to claim 2, wherein the control signals are generated on the basis of one input signal.

4. The memory according to claim 3, wherein at least one of the control signals is generated by level shifters.

5. The memory according to claim 1, wherein the MOS transistors comprises

a thin film type transistor which short-circuits

the two power supply nodes, and

a thick film type transistor which has a gate oxide film thicker than that of the thin film type transistor and applies a precharge potential to the two power supply nodes.

6. The memory according to claim 5, wherein the thin film type transistor is adjacent to the sense amplifier, and the thick film type transistor is adjacent to the bit line equalizer.

7. The memory according to claim 6, wherein isolation areas are arranged respectively between the thin film type transistor and the thick film type transistor and between the sense amplifier and the bit line equalizer.

8. The memory according to claim 7, wherein

the sense amplifier comprises a thin film type transistor, and

the bit line equalizer comprises a thick film type transistor which has a gate oxide film thicker than that of the thin film type transistor.

9. A semiconductor memory comprising:

a memory cell array comprising memory cells arranged in a matrix;

sense amplifiers to read/write data from/in the memory cell array;

pairs of bit lines to connect the memory cells to the sense amplifiers;

bit line equalizers to equalize potentials of the pairs of bit lines; and

a sense amplifier equalizer to equalize potentials of two power supply nodes for at least one of the sense amplifiers,

wherein the sense amplifier equalizer comprises MOS transistors whose gate oxide films have different thicknesses.

10. The memory according to claim 9, wherein the sense amplifier equalizer is arranged between the sense amplifiers.

11. The memory according to claim 9, wherein the sense amplifier equalizer is controlled by control signals having different logic amplitudes in correspondence with the MOS transistors.

12. The memory according to claim 11, wherein the control signals are generated on the basis of one input signal.

13. The memory according to claim 12, wherein at least one of the control signals is generated by level shifters.

14. The memory according to claim 11, wherein the MOS transistors comprises

a thin film type transistor which short-circuits the two power supply nodes, and

a thick film type transistor which has a gate oxide film thicker than that of the thin film type

transistor and applies a precharge potential to the two power supply nodes.

15. The memory according to claim 14, wherein the thin film type transistor is adjacent to one of the sense amplifiers, and the thick film type transistor is adjacent to one of the bit line equalizers.

16. The memory according to claim 15, wherein isolation areas are arranged respectively between the thin film type transistor and the thick film type transistor and between the sense amplifiers and the bit line equalizers.

17. The memory according to claim 16, wherein

each of the sense amplifiers comprises a thin film type transistor, and

each of the bit line equalizers comprises a thick film type transistor which has a gate oxide film thicker than that of the thin film type transistor.